

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	10/801,893	
			Filing Date	March 16, 2004	
			First Named Inventor	Gi-ho Park	
			Group Art Unit	2187	
			Examiner Name	Than Vinh Nguyen	
Sheet	1	of	A1	Attorney Docket Number	5649-1159

U.S. PATENTS AND PATENT PUBLICATIONS					
Examiner Initials*	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code (if known)		
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FOREIGN PATENT DOCUMENTS							
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OTHER NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
/T.N./	1.	Ghose et al. "Reducing Power in Superscalar Processor Caches Using Subbanking, Multiple Line Buffers and Bit-Line Segmentation" <i>Proceedings Of The 1999 International Symposium On Low Power Electronics And Design</i> pp. 70-75 (1999)	
/T.N./	2.	Hennessy et al. <i>Computer Architecture: A Quantitative Approach</i> , 3 rd Edition, chapter 3.11 "Another View: Thread-Level Parallelism" Morgan Kaufmann Publishers, San Francisco, CA (2003)	
/T.N./	3.	Kin et al. "The Filter Cache: An Energy Efficient Memory Structure" <i>Proceedings of the Thirtieth Annual IEEE/ACM International Symposium on Microarchitecture</i> , pp. 184-193, (1997)	

Examiner Signature	/Than Nguyen/	Date Considered	07/16/2007
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.